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# WinHEC 99

Windows® Hardware Engineering Conference

# **Future PC System Architecture - Internal**

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# **Agenda: Generations of the PC Architecture**

- ◆ **6th Generation**
  - ◆ **Instruction set modernization**
  - ◆ **Enhancement of legacy**
- ◆ **7th Generation**
  - ◆ **Revolution in data movement**
  - ◆ **μArchitecture to utilize instruction set**
  - ◆ **Completes migration of server & workstation features to mainstream PCs**

# **Instruction Set Modernization**

- ◆ **Multimedia Content Provided Motivation**
  - ◆ **SIMD provides performance opportunity**
  - ◆ **Brings vector processing to the desktop**
- ◆ **MMX™ Instructions Opened the Door**
- ◆ **3DNow!™ Technology solves the Real Problem**
  - ◆ **Geometry, audio, physics**
- ◆ **Enhanced MMX For Video Helps Integer**
- ◆ **Microsoft will Support these Technologies in Future Releases of Visual Studio**



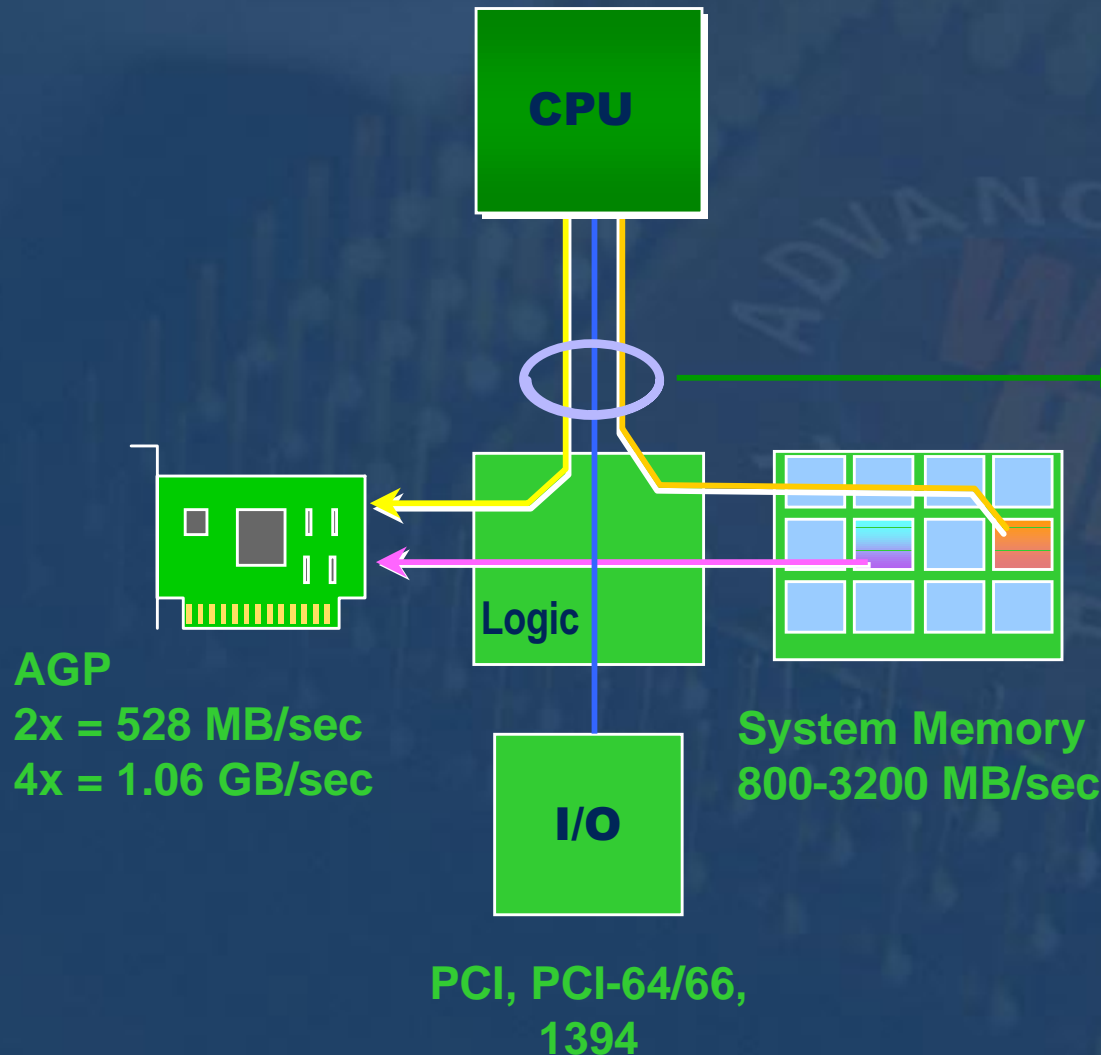
# 6th Generation: Extensions of Legacy Architecture

- ◆ **Socket 7 Evolved to:**
  - ◆ **Super7™ (100MHz, AGP2X)**
  - ◆ **Slot 1 (100MHz, AGP2X, partial split transaction)**
  - ◆ **Camino (133MHz, AGP4X)**
- ◆ **Caches Evolved: Large L1, Back side L2:**
  - ◆ **AMD-K6®-III: 32KB/32KB/256KB (full speed)**
  - ◆ **Pentium® III: 16KB/16KB/512K (half speed)**

# **The 7th Generation**

**Completion of Server &  
Workstation Migration to  
Mainstream PC**

# Data Bandwidth Deficit



## Today's Simplified Maximum Bandwidth Requirements:

- Memory (8 x 100) = 800 MB/s
- 2x AGP (2 x 32 x 8) = 528 MB/s
- PCI (4 x 32) = 133 MB/s
- Total = 1,461 MB/s**

## Tomorrow's Simplified Maximum Bandwidth Requirements:

- Memory (2 x 800) = 1.6 GB/s
- 4x AGP (4 x 8 x 33) = 1.1 GB/s
- I/O (various) ~ .5 GB/s
- Total ~ 3.2 GB/s**

## 6th Generation Front side bus:

**Today: 8 x 100 = 800 MB/sec**  
**Q3'99: 8 x 133 = 1.06 GB/sec**

# The Data Problem

- ◆ **Data Bottlenecks**
  - ◆ **Slow Legacy processor buses**  
(.8 to 1.06 GB/s)
  - ◆ **Shared buses for MP**
  - ◆ **Small (32 byte) cache blocks**
  - ◆ **Limited I/O bandwidth**
- ◆ **Technology Advances**
  - ◆ **500MHz processors today; 1GHz in 2000**
  - ◆ **SIMD processes data faster**
  - ◆ **1394, 4x AGP, etc.**
  - ◆ **Increasing snoop traffic**

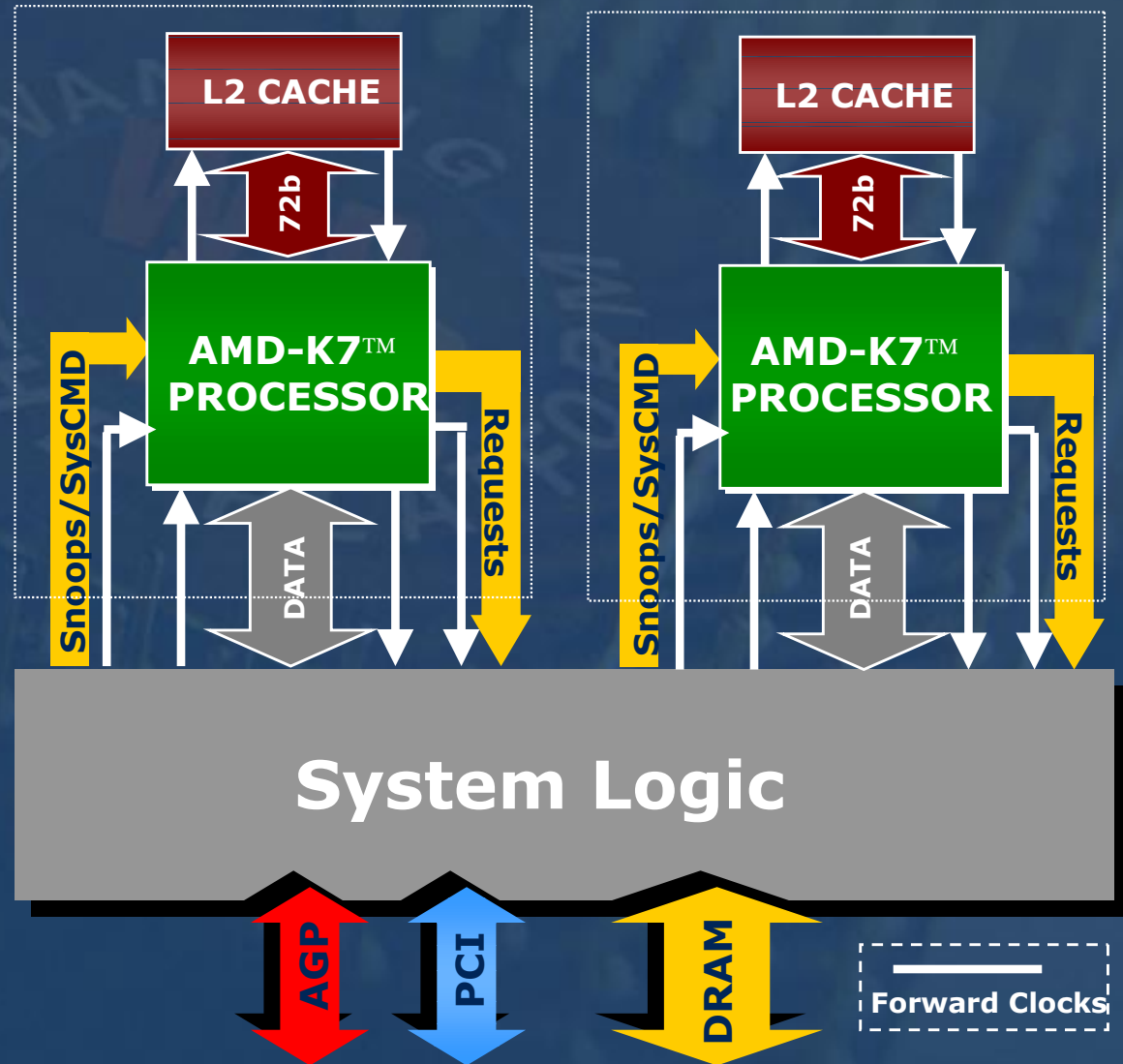


# The Solution: A Revolution in Data Movement

- ◆ **AMD-K7 Fully Programmable Back Side L2:**
  - ◆ Scales beyond  $8\text{B} * 1\text{GHz} = 8 \text{ GB/s}$
- ◆ **AMD-K7 Front Side Bus Options**
  - ◆  $8\text{B} * 133 \text{ MHz} = 1.1 \text{ GB/s}$
  - ◆  $8\text{B} * 200 \text{ MHz} = 1.6 \text{ GB/s}$
  - ◆  $8\text{B} * 266 \text{ MHz} = 2.1 \text{ GB/s}$
  - ◆  $8\text{B} * 400 \text{ MHz} = 3.2 \text{ GB/s}$
- ◆ **Memory Bandwidth**
  - ◆ **SDRAM:**  $8\text{B} * 100 \text{ MHz} = 0.8 \text{ GB/s}$   
 $8\text{B} * 133 \text{ MHz} = 1.06 \text{ GB/s}$
  - ◆ **Rambus:**  $2\text{B} * 400 \text{ MHz} * 2\text{x} = 1.6 \text{ GB/s}$

# AMD-K7™ Front side Bus: EV6 in a PC

- ◆ 1.6GB/s that scales to 3.2GB/s per Processor
- ◆ Back Side L2 Cache
- ◆ Up to 24 Outstanding Transactions per Processor
- ◆ 13-Pin Address Bus
- ◆ 13-Pin Snoop Bus
- ◆ 72-Pin Data Bus w/ECC
- ◆ Scales to 43-bit Physical Address

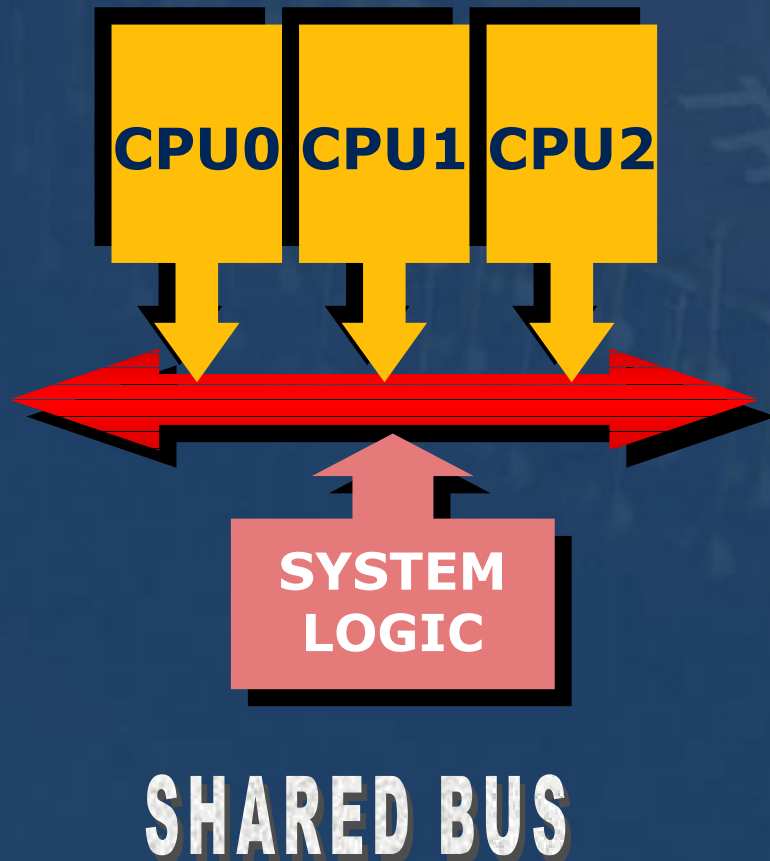


# Server Level MP Support

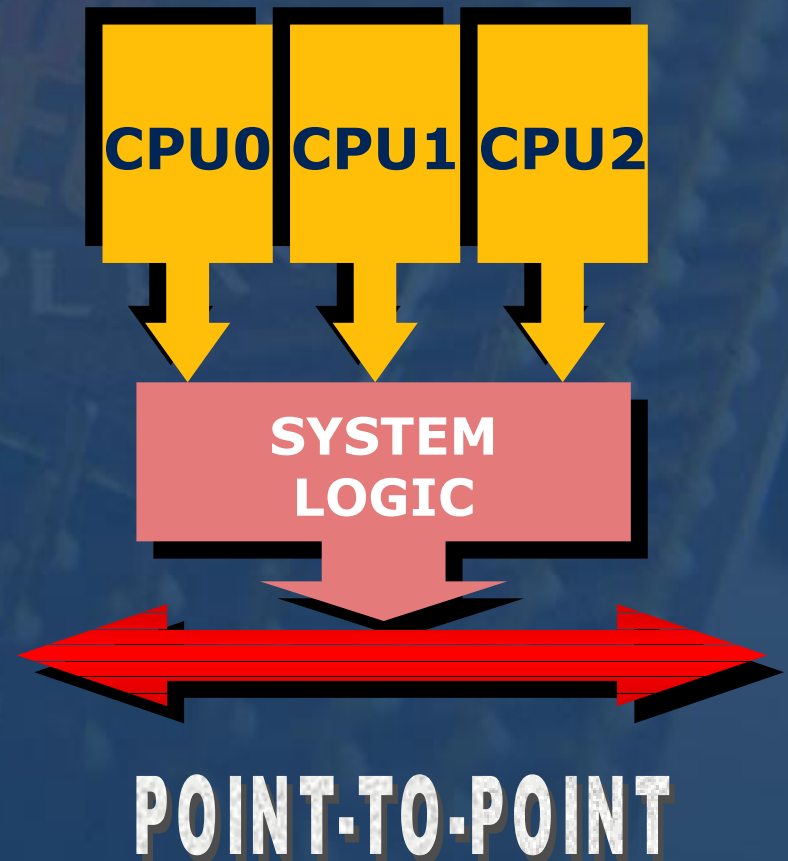
- ◆ **Separate Data, Address, and Snoop Paths**
- ◆ **Point-to-Point access to Data Bus in MP Configuration(s)**
- ◆ **True Split Transaction Bus**
  - ◆ **Up to 24 outstanding operations per AMD-K7 processor**
- ◆ **Scales to 8 Terabytes of Data Space**

# Bus Topology Comparison

- Shared bus limits frequency
- Available bandwidth is shared
- Snoops interferes with Xfrs



- PTP source synchronous bus
- Independent bus per CPU
- Separate path for snoop traffic

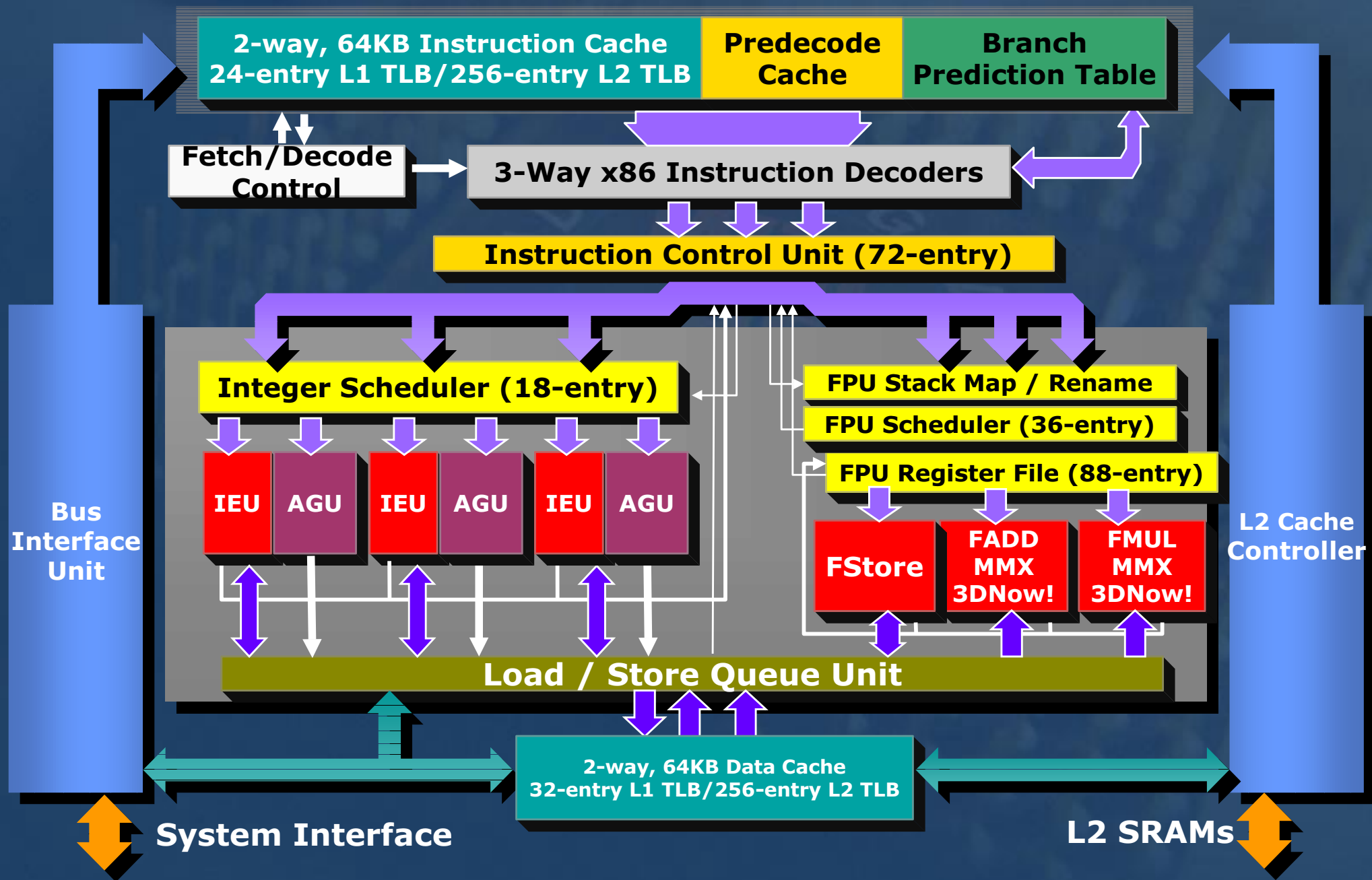


# **Workstation Class Floating Point & Multimedia Performance**

- ◆ **7th Generation Data Bandwidth Enables 7th Generation Execution Performance**
- ◆ **9 Issue Total Execution Bandwidth**
- ◆ **3 Issue Floating Point Unit**
  - ◆ **2x increase in peak execution rate**
  - ◆ **Multiply, add, control/move/store ops**
  - ◆ **No switching overhead:**
    - 3DNow!/MMX <> x87 code**
- ◆ **Deep Out Of Order Window**
  - ◆ **36 Entry FPU scheduler**
  - ◆ **72 Entry ROB**



# AMD-K7™ Microarchitecture



# Summary

- ◆ **The 7th Generation Revolution Begins this Summer**
  - ◆ **1.6 GB/s data bus bandwidth**
  - ◆ **Performance jump in floating point**
- ◆ **And It Supports:**
  - ◆ **Doubling the bandwidth in the memory system**
  - ◆ **Huge increases in frequency**
  - ◆ **Further increases in the data bus bandwidth**
  - ◆ **Much greater I/O bandwidth that isn't bottlenecked on the system bus (4x AGP, 64/66 PCI)**
  - ◆ **AMD-K7™ Processor Enables the 7th Generation**



# Call to Action

- ◆ **Platform Innovation Can Begin Now**
  - ◆ **Develop chipsets, graphics, and memory systems for the 7th Generation PC**
  - ◆ **Enhance I/O subsystems**

**Enables:**

- ◆ **ISV's to Develop the Next Generation of Killer Applications**

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